IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

1. - 18. (Cancelled)

19. (New) Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator, including a plurality of elements tuned by the voltage controlled oscillator, the method comprising:

comparing an output signal of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage controlled oscillator operating mode, using a linearized frequency versus voltage curve, in a first frequency tuning operation enabling a wide locking range, to a linear high gain mode; and

automatically switching, after locking to an appropriate frequency with the said first tuning operation, said voltage controlled oscillator operating mode to a zero-gain mode, while keeping the frequency of said voltage controlled oscillator unchanged.

20. (New) Method according to claim 19, wherein, after said zero-gain mode, said voltage controlled oscillator operating mode is switched to a low gain mode enabling a fine tuning of the frequency by the phase locked loop for compensating small residual frequency errors and temperature variations.

21. (New) Method according to claim 19, wherein the linearization of the voltage controlled oscillator frequency versus voltage operating curve comprises:

breaking the required linear frequency versus voltage curve into several sections over either constant or non constant voltage intervals;

selecting for each section a corresponding element tuned by the voltage controlled oscillator giving the same frequency variation over said section; and

submitting each element tuned by the voltage controlled oscillator to a specific voltage, deduced from the loop filter output tuning voltage, in such way that said element is activated in the same voltage interval as its corresponding section.

22. (New) Method according to claim 19, wherein the linearization of the voltage controlled oscillator

frequency versus voltage operating curve is performed during the linear-high gain mode.

23. (New) Method according to claim 19, wherein the switching operation of the voltage controlled oscillator from the linear-high-gain mode to the zero-gain mode comprises:

isolating the elements tuned by the voltage controlled oscillator from their controlling voltages when the phase locked loop is locked;

comparing each element tuned by the voltage controlled oscillator voltage to a reference voltage to determine if the value of said element was at it maximum or its minimum when the phase locked loop was locked;

depending on the result of this comparison, applying a voltage equal to a specified minimum value or to a specified maximum value to each element tuned by the voltage controlled oscillator, switching its value to its maximum or to its minimum, the total value of said element is thus equal to their value when the phase locked loop was locked; and

freezing the elements tuned by the voltage controlled oscillator in the state previously obtained to activate thus the zero-gain mode for the voltage controlled oscillator.

24. (New) Method according to claim 20, wherein the switching operation of the voltage controlled oscillator from the zero-gain mode to the low-gain mode comprises:

using an additional element tuned by the voltage controlled oscillator that is dimensioned to achieve the needed fine tuning with a low voltage controlled oscillator gain;

linking said element tuned by the voltage controlled oscillator to a fixed voltage during linear-high-gain mode and zero-gain mode;

isolating said additional element from this fixed voltage during the switching step from zero-gain mode to low-gain mode;

linking said additional element to the tuning voltage supplied by the loop filter of the phase locked loop; and

achieving the fine tuning operation by the phase locked loop.

25. (New) Method according to claim 20, wherein the loop filter output voltage is compared to an upper and a lower limit by means of additional comparators during low gain mode; and the tuning operations are restarted and the initial linear high gain mode is selected again when the loop filter output voltage reaches either of the upper limit or the lower limit.

26. (New) Method according to claim 19, wherein the phase locked loop locking time during the linear high gain mode is improved by switching off a fraction of the capacitance of the loop filter or optionally by increasing the current of the charge pump.

27. (New) Method according to claim 20, wherein the phase locked loop stability during the operations at the linear high gain and the low gain modes is preserved by decreasing the charge pump current during the linear high gain mode and by increasing said current during the low gain mode in such way that the product of the charge pump current and the gain of the voltage controlled oscillator remains constant.

28. (New) Integrated circuit, comprising:

a phase locked loop circuit including,

a detector to compare the phase and frequency of a reference signal to the phase and frequency of an internal feedback signal and to generate output error signals,

a charge pump to generate amounts of charges proportional to said output error signals,

a loop filter to set an analogue voltage proportional to the charges accumulated in their capacitors,

a voltage-controlled oscillator with multiples inputs corresponding each to an element tuned by the voltage controlled oscillator, and

a gain mode switcher circuit connected between the loop filter output and the voltage-controlled oscillator inputs, to enable the voltage-controlled oscillator to work successively in a linear high-gain mode and a zero-gain mode, the gain mode switcher circuit including,

offsets generators to generate the voltages after shifting the loop filter output voltage with predefined offsets,

comparators, and

a switch configuration to apply the voltages of the offset generators to the inputs of the voltage-controlled oscillator during the linear high gain mode, to isolate the inputs of the voltage-controlled oscillator from the offset generators and to apply the output voltages of said offsets generators to the inputs of the comparators during the transition to zero gain mode, to apply the resulting outputs voltages of said comparators to the inputs of the voltage-controlled oscillator, and to finally freeze the state of each comparator and thus the frequency of the voltage-controlled oscillator, making it independent on the loop filter output voltage, which constitute the zero-gain mode.

29. (New) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the elements tuned by the voltage controlled oscillator include varactors dimensioned in such a way that the voltage controlled oscillator has a relatively constant voltage to frequency gain during the linear high gain mode step, each varactor being controlled by a corresponding input of the voltage-controlled oscillator.

30. (New) Integrated circuit comprising a phase locked loop circuit according to claim 29, wherein the voltage-controlled oscillator further comprises, an additional varactor that enables to achieve a fine frequency tuning during the low gain mode and a switch configuration enabling the application of a constant voltage to said varactor during the linear high gain mode and the zero gain mode, and the application of the loop filter output voltage to said varactor during the low gain mode.

31. (New) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the voltage controlled oscillator is constituted by a current controlled oscillator which include elements tuned by the voltage controlled oscillator comprising voltage to current converters

including voltage controlled current sources dimensioned in such way that the current controlled oscillator has a relatively constant voltage to frequency gain during the linear high gain mode step, each controlled current sources being controlled by a corresponding input of the voltage-controlled oscillator.

32. (New) Integrated circuit comprising a phase locked loop circuit according to claim 31, wherein each element tuned by the voltage controlled oscillator further comprises, an additional controlled current sources that enables to achieve a fine frequency tuning during the low gain mode and a switch configuration enabling the application of a constant voltage to said controlled current sources during the linear high gain mode and the zero gain mode, and the application of the loop filter output voltage to said controlled source during the low gain mode.

33. (New) Integrated circuit comprising a phase locked loop circuit according to claim 28, further comprising a lock detector that activates the switch configuration in such way that: the linear high gain mode is selected during a sufficiently long time for the loop to lock and the transition to zero gain mode is activated after this locking.

34. (New) Integrated circuit comprising a phase locked loop circuit according to claim 30, further comprising comparators that set an upper and a lower limit for the loop filter output voltage during the low gain mode and restart the initial linear high gain mode when said loop filter output voltage reaches either of these two limits.

35. (New) Integrated circuit comprising a phase locked loop circuit according to claim 28, further comprising a voltage doubler circuit that increase the voltage supply of the charge pump, the loop filter and the offsets generators during the linear high-gain mode and hence enhance the tuning range of the phase locked loop circuit.

36. (New) Integrated circuit comprising a phase locked loop circuit according to claim 35, further comprising a switch configuration enabling the application of the voltage doubler to the charge pump, the loop filter and the offsets generators during the linear high-gain mode and the output operating voltage supply during the low gain mode.